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Phase Distortion Mechanism of a GaAs FET Power Amplifier for Digital Cellular Application

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ABSTRACT

A conventional class AB amplifier with high efficiency has had phase distortion which is not suitable for π/4-shift QPSK signal. A simple FET model including four non-linear elements is presented to explain the distortion mechanism. By using those parameters, a class AB amplifier with low phase variation of less than 2 degrees is designed.

I. INTRODUCTION

Digital mobile radio services using π/4-shift QPSK signal are planed to start in Japan and then in the U.S. In order to deal with π/4-shift QPSK signal without distortion, a linear amplifier is required. Though an amplifier operating in class AB mode is more efficient than in class A mode, a conventional class AB amplifier has a phase distortion problem for π/4-shift QPSK signal.

Studies on some large signal GaAs FET models [1][2] and analysis of large signal GaAs FET amplifier characteristics [3] have been reported. Recently, Parra designed a low distortion GaAs FET power limiter [4]. He pointed out from his experimental results that reverse gate current played important role in phase variation. However, the detail of the mechanism was not described.

In this paper, a new non-linear GaAs FET model, instead of the conventional large signal GaAs FET model, is presented incorporating the phase distortion mechanism in a class AB amplifier. From the results of the analysis, the authors designed a low phase distortion power amplifier by optimizing circuit parameters and device parameters.

II. EXPERIMENTAL RESULTS OF PHASE CHARACTERISTICS

(A) *INPUT-OUTPUT CHARACTERISTICS*

First, input-output characteristics of a conventional GaAs-FET amplifier in class AB (10% Idss) mode, fabricated by using stub-tuners, was measured. The output power of the amplifier was 2W at saturation under 6V dc bias operation.

Figure 1 shows the measurement results of input-output characteristics. It shows a phase variation in accordance with input power levels. The phase variation over 10 degrees would cause distortion expected to degrade π/4-shift QPSK signal.

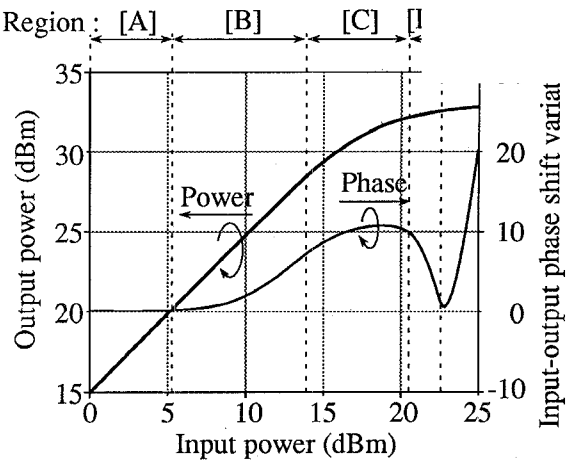

Fig. 1 Measured output power and phase of the conventional class AB power amplifier (at 950 MHz).

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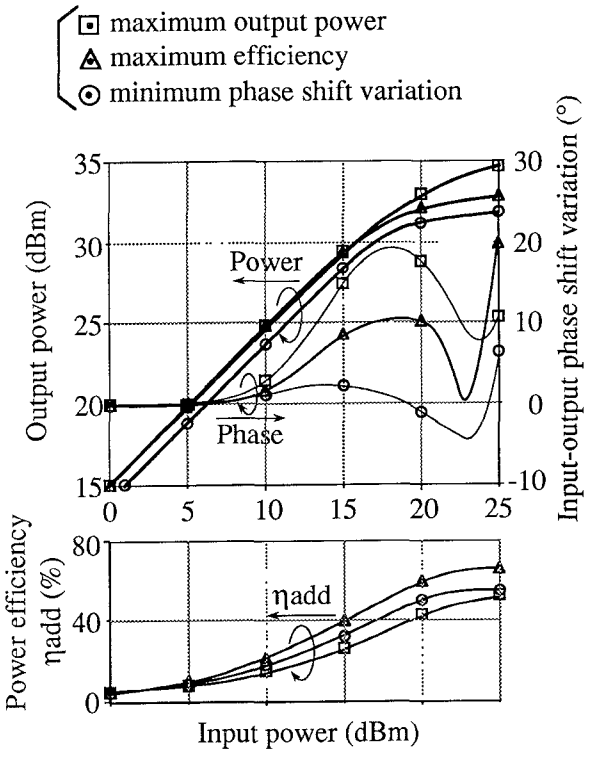
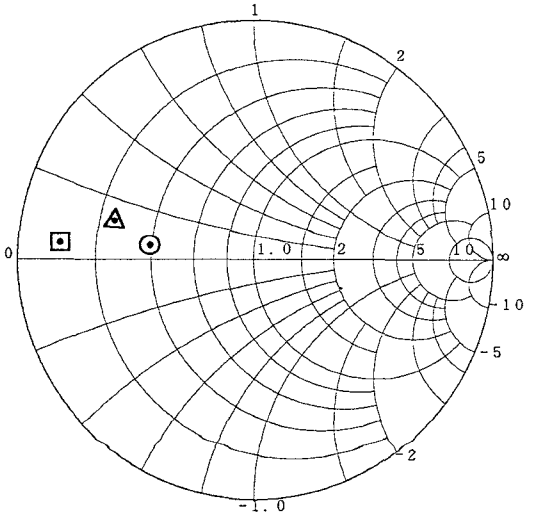


(a) Measured phase, output power and efficiency versus input power.



(b) Corresponding load impedances measured.

Fig. 2 Measured output performances with respect to the variation of load impedance.

(B) *EFFECTS OF LOAD IMPEDANCE*

By changing load impedances, phase variations are examined for the class AB amplifier. Figure 2(a) shows measurement results of phase variations versus load impedances, while Figure 2(b) shows corresponding load impedances. They show that the optimum load impedances for maximum output power, maximum efficiency and minimum phase variation are different from each other.

III. ANALYSIS OF FET MODEL

(A) *LARGE SIGNAL FET MODEL*

In order to explain the phase characteristics of an FET, the authors present a conceptual equivalent circuit of power FET shown in Figure 3 which is modified from the conventional non-linear model[1]. Although it is restricted to an equivalent expression of phase performance, it can make clear understanding of the phase characteristics.

In this model, three non-linear conductances and one non-linear capacitance are included. They are gate-source conductance, gate-drain conductance, drain-source conductance and gate-source capacitance. For every frequency spectrum and dc, the linear elements in the equivalent circuit have different values calculated by Fourier transform. And only ones for the fundamental wave are required to explain the phase distortion phenomena. Thus, in this model, each non-linear element is expressed as an equivalent linear element in the fundamental frequency.

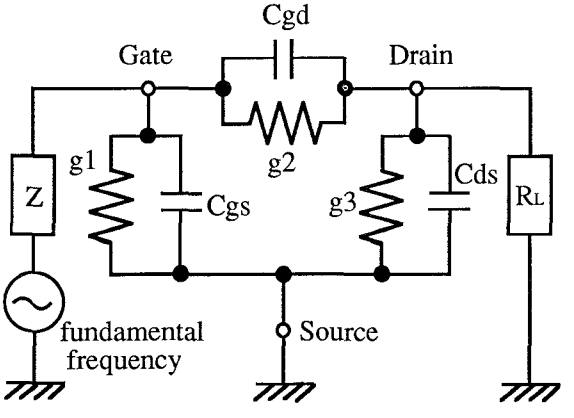


Fig. 3 Large-signal FET model using four non-linear elements. (describing phase performance)

Next, element value variations depending on rf input power and dc bias voltage can be explained as follows.

(1) Gate-source conductance g1 is very small and can be ignored when gate-source voltage Vgs is negative and does not reach gate-source breakdown voltage. When Vgs is positive, gate-source current flows and g1 must be very large. Figure 4 shows measured gate currents versus input power levels with the horizontal axis the scale of which is the same as that in Figure 1. g1 becomes large in Region E.

(2) Gate-drain conductance g2 is related to gate-drain breakdown voltage and increases in accordance with gate-drain leak current. This part is corresponding to Region C, D and E.

(3) Gain is the function of drain-source conductance g3. To discuss the relation between g3 and gain, we employ a small signal equivalent circuit expression of Figure 5. From this, the gain G is obtained as

$$G = \frac{Rin}{R_L} \bullet \left(\frac{R_L}{1+g3 \bullet R_L}\right)^2 \bullet gm^2$$

where Rin refers to input resistance. In assumption that gm is constant, it can be said that g3 increases when gain is compressed.

(4) Gate-source capacitance Cgs is small if gate-source voltage Vgs is negative in the proximity of gate pinch-off voltage [1].

Gate-drain capacitance Cgd and drain-source capacitance Cds are assumed to be constant. Figure 6 illustrates phase shift variation of the equivalent circuit with respect to g1, g2, g3 and Cgs. Output phase leads the input phase if g1 or g3 becomes large and it lags if g2 or Cgs becomes large.

(B) *ANALYSIS OF AMPLIFIER PHASE CHARACTERISTICS*

From the presented FET model, the results shown in Figure 1 is examined in terms of phase characteristics. The analysis may be subdivided into five regions with respect to input power levels: (see Figure 1 and 4).

Region A : The amplifier is operating in class A mode and gain is constant. Signal is small. Gate current nearly equals zero. Phase does not change because no element values in the circuit are changed.

Region B : Input peak voltage reaches near gate pinch-off and the gain goes down gradually. Phase goes ahead because g3 increases.

Region C : In addition to change of g3, gate-drain leak current increases. Phase goes behind, because g2 increases.

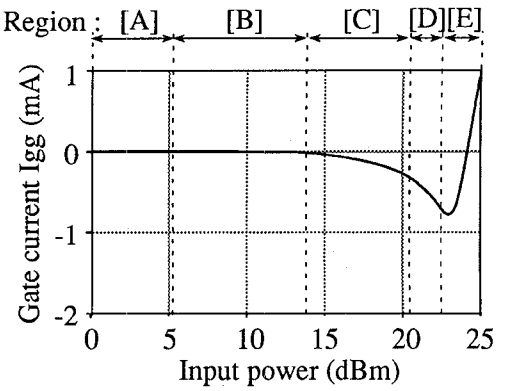


Fig. 4 Measured gate current versus input power.

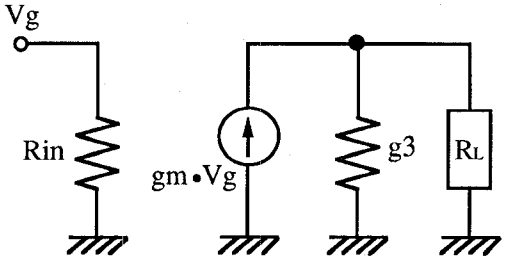


Fig. 5 Specialization from a small-signal equivalent circuit expression.
(describing gain performance)

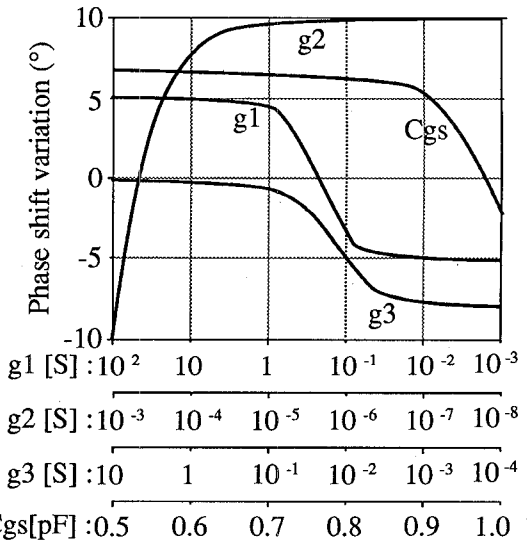


Fig. 6 Calculated phase shift variation versus g1, g2, g3 and Cgs.

Region D : Gate-source capacitance Cgs increases. Phase goes far behind.

Region E : Gate-source voltage Vgs swings over positive. Phase goes ahead rapidly, because g1 increases quickly. This region has little to do with g3, g2 and Cgs.

IV. DESIGN EXAMPLE OF LOW DISTORTION AMPLIFIER

From the results, it is learned that the phase variation could be canceled by combining the effect of g2 and the effect of g3. Thus, the load impedance and the gate bias resistance is designed so that the gate bias point can shift depending on breakdown leak current. Input-output characteristics of the designed amplifier is shown in Figure 7. Phase variation less than 2 degrees is obtained.

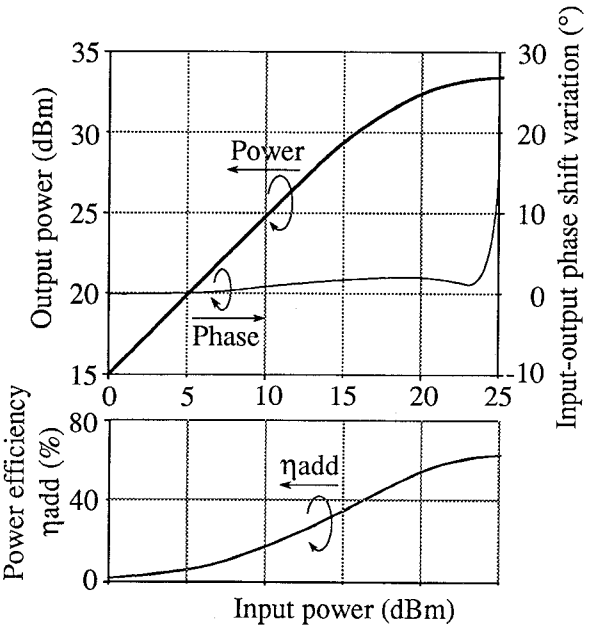


Fig. 7 Measured output performances of the class AB power amplifier designed for low phase distortion (at 950 MHz).

V. CONCLUSION

A simple FET model explaining the phase distortion mechanism of GaAs-FET power amplifiers is presented. The model includes three non-linear conductances and one non-linear capacitance. The behavior of those elements is analyzed in detail. By using the results from the analysis, the amplifier with phase variation of less than 2 degrees is designed.

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